REMARKS

Claims 109-112, 115, 116, 119, 120, 123, 127 and 129-135 are pending. Claims 109, 111, 115 and 132 are amended.

As a preliminary matter, an Information Disclosure Statement is filed herewith citing references made of record in related application S.N. 09/766,656 and 09/635,124, which have not yet been made of record in the present application.

Claims 132 and 133 were rejected under 35 USC §112, first paragraph. These claims have been amended to delete reference to the phrase objected to by the Examiner. Accordingly, it is believed that the presently pending claims are in full compliance with 35 USC §112.

Claims 109-112, 131, 134 and 135 were rejected under 35 USC §102(e) as being anticipated by Yasunaga. Favorable reconsideration of this rejection is earnestly solicited.

Independent claims 109 and 111 have been amended to specify that the resin layer is a compression molded resin layer. Yasunaga does not teach or suggest this feature.

A resin layer formed by a compression-molding process provides uniform and superior characteristics when used as a thin resin layer covering the entire wafer surface formed with projection electrodes as compared with the resin layer formed by a transfer molding process. This is because a sealing resin generally contains glass particles called filler having a diameter of 10-20 microns in an epoxy resin with a proportion of 80-90 weight percent for increasing strength and decreasing linear thermal expansion coefficient.

In the case of forming a thin resin layer on the entire wafer surface by a transfer molding process, a gap corresponding to the thickness of the resin layer to be formed is set between the wafer and the mold and injection of resin is conducted from the periphery of the wafer. In the

case of forming a resin layer of 100 micron thickness on a wafer of 20cm diameter, the resin is injected through a gap having a size of 100 microns. This resin has to be spread over the entire surface of the 20cm diameter wafer.

In the case of spreading in such a narrow and elongated space and filling the space with the resin, it is effective to decrease the viscosity of the resin. It is possible to reduce the viscosity of a resin by reducing the content of the filler. However, such a decrease of filler content invites a decrease of strength of the resin layer and an increase of linear thermal expansion coefficient. Thus, because of the increased thermal expansion coefficient difference between the silicon wafer and the resin layer formed thereon, there arises a problem that the wafer undergoes warping and handling of the wafer becomes difficult. Further, the strength of the final package is degraded, leading to poor device performance.

There also arises the problem that the protection electrodes formed on the entire wafer surface prevent uniform distribution of the fillers. Because the gap through which the resin is injected is small, there can be a case in which the projection electrodes formed on the wafer surface disturb the uniform flow of the fillers at the time the injected resin is spread inside the mold space. When this is the case, there arises a non-uniform filler distribution such that a large number of the filler particles are accumulated in the resin part near the injection port and the filler content decreases with distance from the resin injection port. Thereby, the resin layer shows non-uniformity on the wafer surface and there can be a weak resin part depending on the location of the wafer surface. Further, there may be cases in which the thermal expansion coefficient is deviated from the intended thermal expansion coefficient depending on the location of the wafer. Thereby, the reliability of the semiconductor device is deteriorated seriously.

In the case of the compression molding process the sealing resin is spread over the entire wafer surface when forming a resin layer, by compressing the resin by conducting a process of decreasing the volume inside the cavity by closing together the upper mold and the lower mold. The resin tablet put on the wafer at the beginning of the molding process had a height of 10-15mm, and thus, there exists a distance of 10000-15000 microns between the wafer surface and the upper mold at the beginning of the molding process. This distance is larger by 100 times or more as compared with the gap size used in the transfer molding process. This distance is decreased with the progress of the molding process and becomes equal to the thickness of the resin layer such as 100 microns at the end of the resin molding process.

Further, in the case a resin tablet is placed at the center of the wafer, the distance needed for the resin to flow for covering the entire wafer surface is reduced to 10cm in the case of a 20cm diameter wafer, while this flow distance is one-half of the distance needed for the resin to flow in the case of using the transfer molding process.

Thus, in the case of compression molding process, the gap in which the resin is caused to flow is increased and the distance needed for the resin to flow is decreased. Thereby, it becomes possible to use a high viscosity resin containing a high proportion of fillers and it becomes possible to distribute the fillers uniformly over the entire resin, irrespective of the protruding electrodes formed on the wafer surface. With this, a compression-molded resin layer maintains a uniform resin strength irrespective of the location on the wafer.

Because the resin layer can be formed uniformly within the range of desired thermal expansion coefficient by using a compression-molded resin layer, the present invention can provide highly reliable semiconductor devices with high yield.

Because the resin layer formed by the compression molding process is different from the resin layer of the prior art in terms of uniformity and reliability, the semiconductor device using the compress molded process should be distinguished over the semiconductor device of the prior art.

Claims 115, 116, 119 and 120 were rejected under 35 USC §103(a) as being unpatentable over the combination of Karnezos and Yasunaga. It is the Examiner's position that the conductive films 50c and 46c form a common electrically conductive film.

Claim 115 has been amended in a manner similar to claim 119, i.e., to specify a part of said protruding electrode sealed by said resin layer and said end portion are covered with a common electrically conductive film. Contrary to the assertion of the Examiner, Karnezos fails to teach the claimed common electrically conductive film since the Examiner relies upon a teaching both a film 50c and a film 46c, which clearly are not the same film.

Claims 123, 127, 129 and 130 were rejected under 35 USC §102(b) as being anticipated by Brooks et al. In this rejection, the Examiner argues that Brooks et al. would inherently possess the structural characteristic imparted by "compression-molded." This rejection is respectfully traversed.

There is no teaching or suggestion of compression molded provided by Brooks et al. Since Brooks et al. does not teach compression molding, Brooks et al. can not be considered to anticipate the claims. See the above-discussion regarding the differences in regard to compression molding.

Claims 132 and 133 were rejected under 35 USC §103(a) as being unpatentable over Brooks et al. Favorable reconsideration of this rejection is respectfully requested.

From the Examiner's description, the Examiner appears to rely on Figs. 2-5 of Brooks et al. In any event, the claims have been amended to specify the feature of a compression molded resin layer. Accordingly, for the above reasons, Brooks et al. fails to teach or suggest the claimed invention.

It is noted that the Examiner acknowledges that Brooks et al. does not teach that a sidewall surface of the semiconductor element is exposed and a sidewall surface of said semiconductor device. To remedy this deficiency, the Examiner argues that it would have been obvious to combine the second embodiment of Brooks et al. with the first embodiment "because it would facilitate mass production." Although the facilitation of mass production would appear to provide motivation, Brooks et al. does not teach or suggest that such a combination would result in facilitation of mass production. The first and second embodiments of Brooks et al. are distinct from each other. There is no basis for the Examiner's allegation that combining the first and second embodiments of Brooks et al. would facilitate mass production.

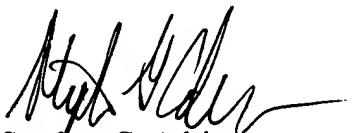
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



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Attachments: Petition for Extension of Time
Information Disclosure Statement